PROCESS TO MINIMIZE AND/OR ELIMINATE CONDUCTIVE MATERIAL COATING OVER THE TOP SURFACE OF A PATTERNED SUBSTRATE AND LAYER STRUCTURE MADE THEREBY

This application claims the priority of U.S. provisional application no. 60/198,371, filed April 19, 2000, the disclosure of which is expressly incorporated by reference herein.

BACKGROUND AND SUMMARY OF THE INVENTION

Multi-level integrated circuit manufacturing requires many steps of metal or metal alloy and insulator film depositions followed by photoresist patterning and etching or other material removal operation. After photolithography and etching, the resulting wafer or substrate surface is non-planar and contains many features such as vias, lines or channels, test pads and bond pads. Often, these features need to be filled with a specific material such as a metal, and then the wafer topographic surface needs to be planarized, making it ready for the next level of processing.

Electrodeposition is a widely accepted technique for depositing a highly conductive material such as copper (Cu) into the features on the semiconductor wafer surface. Chemical mechanical polishing (CMP) is then employed to planarize the resulting surface and to polish the conductive material off of the field regions of the surface, leaving the conductive material only

within the features themselves. Another approach by which the excess metal can be removed from the wafer surface is electro-polishing, which is often also referred to as "electrochemical etching" or "electro-etching". Chemical etching can also be used to remove the excess metal or other conductive material. In chemical etching, the material to be removed from the wafer surface is brought into contact with an etching solution. A chemical reaction between the etching solution and the material causes dissolution of the material and removal of the material from the wafer surface. In electro-polishing, both the material to be removed and a conductive electrode are dipped into an electro-polishing electrolyte. Typically, an anodic (positive) voltage is applied to the material with respect to the conductive electrode. With the help of the applied voltage, the material is electrochemically dissolved and removed from the wafer surface. Electro-polishing is generally considered to be more controllable and faster than chemical etching.

Figures 1 through 3 show an example of a prior art procedure used for filling patterned substrate features with electrodeposited Cu and then polishing the deposited Cu, and the substrate, to obtain a structure with a near-planar surface and electrically isolated Cu plugs or wires. In the example shown, the wafer 20 itself forms part of the patterned substrate. The example shown demonstrates an especially challenging case of metal filling and

planarization procedures which are carried out with patterned substrate features having widely different sizes.

In Figure 1, the large feature 1 and the small feature 1s are opened in the insulator layer 2, which is grown on a wafer 20. Of course, the insulator layer could be one which is grown on another previously processed layer rather than the wafer 20. To fill these features with Cu, a barrier/adhesion layer 3 is first deposited over the whole insulator layer and wafer surface, thereby forming a patterned substrate. Then, a conductive Cu seed layer 4 is deposited over the barrier layer 3. By making electrical contact to the seed layer 4 and/or the barrier layer 3, placing the patterned substrate in a Cu plating electrolyte, placing an anode in the same electrolyte, and applying a negative voltage to the seed layer 4 and/or the barrier layer 3 with respect to the anode, Cu is electrodeposited over the whole patterned substrate surface. Figure 2 shows the conductive material on the substrate surface after this plating step. In this conventional approach, the electrodeposited Cu layer 5 forms a very large metal overburden 6 over the top surface of the insulator 2 and over the small feature 1s, whereas, the overburden 6a over the large feature 1 is smaller. The surface region of the insulator 2 over which the Cu overburden is large is also called the "field region". The seed layer 4 is not separately shown in Figure 2; it is rather treated to be an integral part of the Cu film 5.

The surface of the structure in Figure 2 is non-planar and needs to be planarized by removing excess Cu through a polishing step. The Cu overburdens 6 and 6a, and portions of the barrier layer 3 on the field regions, are customarily removed by CMP, yielding the structure in Figure 3, which has a near-planar surface and electrically isolated Cu-filled features. The dishing 7 seen over the large feature 1 of Figure 3 is a commonly observed defect resulting from the CMP step and needs to be minimized or eliminated.

Removal of the large and non-uniform overburden of Figure 2 from the patterned substrate surface and obtaining the structure in Figure 3 with minimal dishing is difficult, time consuming, and expensive. We have recently disclosed methods and apparatus that can plate and polish or minimize accumulation of metal or metal alloy overburden and, therefore, yield a film 8 of conductive material such as Cu, with a uniform overburden 8a as depicted in Figure 4. In this application, we disclose a method that minimizes the thickness of this overburden and even eliminates it through the use of electrochemical etching or chemical etching. In known manufacturing processes, the CMP, chemical etching or electrochemical etching steps are typically carried out in an apparatus separate from the Cu deposition apparatus. One unique feature of the present invention is that all of the process steps are carried out in the same apparatus. This approach further allows

Cu deposition selectively into the features and building up of the Cu overburden only over the features but not over the field regions. Such a structure is very desirable for minimizing dishing during the CMP process as will be explained later.

One prior art process for electrochemical planarization is disclosed in U.S. Patent 5,256,565 to Bernhardt et al. In that process, an already planarized metal film is etched back to the underlying dielectric layer by electro-polishing, ion milling or other procedure. However, this technique requires the use of several steps, i.e. deposition, planarization, and etching, carried out in different apparatus, making it very costly. For example, in the Bernhardt et al. method, Cu deposition is carried out with standard electroplating equipment, which is expected to give a Cu deposit as depicted in Figure 2 of the present application. The metal film is then planarized, using a technique such as CMP, in another machine to obtain a structure such as the one shown in Figure 4 of this application. Bernhardt et al. state that planar Cu films could also be obtained in the electroplating apparatus itself, eliminating the planarization step. However, to get planar Cu deposits in the standard plating apparatus requires deposition of Cu films with thicknesses greater than or equal to half the width of the largest feature on the wafer. This would not be practical in a large category of wafers, which typically contain over 50 micron wide trenches and/or bond or test pads, as well as

features with sub-micron size. Deposition of near-planar Cu films on such substrates would require plating of material which is over 25 microns thick. This is neither practical nor economical.

The last step in the prior art technique disclosed by the Bernhardt et al. patent is the Cu removal step. This step is carried out in a separate electro-polishing or ion etching apparatus. Electro-polishing uses a special electrochemical etching solution in an electro-polishing apparatus. Ion milling requires a separate vacuum system tooled with special means of ion bombarding the substrate surface.

There is a need for the development of high-throughput techniques which can yield planar metal fillings that are formed in the surface features of semiconductor substrates. According to the present invention, such high-throughput techniques involve making, in a single apparatus, a layer structure usable in manufacturing an integrated circuit by performing certain operations. These operations include providing a patterned substrate, supplying an electrolyte solution out of which a conductive material can be plated, under an applied potential, over a surface of the patterned substrate, applying a potential so as to deposit a film of the conductive material out of the electrolyte solution and over the surface of the patterned substrate, and polishing the film of the conductive material as it is deposited. After the conductive material film has been deposited in this manner, the conductive

material is removed from field regions of the patterned substrate while deposits of the conductive material are left in features defined in the patterned substrate. The deposits of the conductive material are then electrically isolated, resulting in the layer structure.

The field regions are regions of an insulator layer forming part of the patterned substrate. In one preferred embodiment of the invention, at least one additional operation of depositing conductive material is performed after removing the conductive material from these field regions and before electrically isolating the deposits. Electro-etching of the conductive material deposited by each additional depositing operation may be performed.

Preferably, the potential is applied between the surface of the patterned substrate and an anode in the electrolyte solution.

The patterned substrate includes an insulator layer and a barrier layer overlying the insulator layer. The field regions are defined on the insulator layer, and the deposits of conductive material are electrically isolated by removing the barrier layer from these field regions.

At least one additional operation of depositing conductive material before electrically isolating the deposits may be performed. The deposits are annealed after the at least one additional conductive material depositing operation.

The process may further include annealing the deposits after

they are electrically isolated. Electrical isolation of the deposits can be performed by chemical mechanical polishing. Removal of the conductive material can be performed by electro-etching the film of the conductive material. According to one feature of the invention, the film is electro-etched by inverting a polarity of the potential which was originally applied to plate the conductive material.

As an alternative to chemical mechanical polishing, electrical isolation of the deposits can be performed by either reactive ion etching or wet etching.

The film of conductive material may be any of Cu, doped Cu, a copper alloy, Pt, Ag, Au, Pd, Ni, a Pb-Sn alloy, a lead-free solderable alloy, and a magnetic alloy. Preferably, the film is deposited out of the electrolyte solution and polished simultaneously.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a partial cross-sectional view of a patterned substrate, having a conductive seed layer provided on a surface thereof, which is to be plated with conductive material.

Figure 2 is a view similar to Figure 1 but showing the patterned substrate after it has been plated with conductive material.

Figure 3 is a view similar to Figure 2 but with overburdens

removed, with electrically isolated deposits of conductive material remaining, and showing a dishing defect.

Figure 4 shows a patterned substrate after it has been plated with a conductive film, with a planar surface, which has been deposited, for example, by way of an electrochemical mechanical deposition tool.

Figure 5 shows an ideal structure similar to that of Figure 4 but with part of the deposited conductive film etched away.

Figure 6 shows an undesirable structure which would result from partially etching away the layer of plated conductive material shown in Figure 2.

Figure 7 shows an ideal structure similar to that of Figure 5 but after further etching such that the deposits of conductive material remaining in features of the patterned substrate are physically isolated from each other.

Figure 8 shows a structure which is similar to that of Figure 7 but after even further etching.

Figure 9 shows the structure of Figure 8 after another deposition operation which builds up the deposits of conductive material.

Figure 10 is a more realistic view of the structure shown in Figure 5.

Figure 11 is a more realistic view of the structure shown in Figure 7.

Figure 12 is a view similar to that of Figure 7 or Figure 11 but showing the grain structure of the deposits of conductive material after annealing.

Figure 13 is a view similar to that of Figure 9 but showing the grain structure of the conductive material deposits after annealing.

Figure 14 shows an annealed conductive material deposit structure, with little or no dishing, obtained by polishing the structure of Figure 13 to electrically isolate the deposits.

Figure 15 is a view of a "bead" structure produced by annealing a different type of plated conductive material.

Figure 16 is a view similar to that of Figure 15 but after the barrier layer has been removed to electrically isolate deposits of the conductive material of Figure 15.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first step of the disclosed process is the deposition of conductive material having a planar surface on the surface of the patterned substrate with features. This can be accomplished by the electrochemical mechanical deposition (ECMD) tool that was previously disclosed by commonly assigned U.S. patent application serial no. 09/201,929, filed December 1, 1998, titled METHOD AND APPARATUS FOR ELECTROCHEMICAL MECHANICAL DEPOSITION. In the present description, Cu is used as an example of the conductive

material to be deposited. However, the invention can be used to deposit other commonly used materials such as doped Cu films, Cu-alloys, Pt, Ag, Au, Pd, Ni, Pb-Sn alloys, Pb-free solderable alloys, magnetic alloys, and others.

In the ECMD method, the deposition electrolyte is fed to a narrow gap between the substrate surface and a pad, which is mounted on or in the near proximity of an anode. The solution makes physical contact to the anode as well as to the substrate surface. The pad, which is typically abrasive, is physically pushed against the substrate surface. Commonly assigned, co-pending U.S. Patent application serial Nos. 09/511,278, filed February 23, 2000, titled PAD DESIGNS AND STRUCTURES FOR A VERSATILE MATERIALS PROCESSING APPARATUS, and 09/621,969, filed July 21, 2000, titled PAD DESIGNS AND STRUCTURES WITH IMPROVED FLUID DISTRIBUTION, relate to certain pad configurations. When the substrate and pad are moved with respect to each other and a negative voltage is applied to the substrate surface with respect to the anode, metal gets plated out of the solution onto the patterned substrate surface and simultaneously gets polished, such that the metal deposition on the field is minimized, to yield the planar structure depicted in Figure 4. One electrolyte chemistry used for such planar metal deposition was disclosed in our recent U.S. Patent application serial No. 09/544,558, filed April 6, 2000, titled MODIFIED PLATING SOLUTION FOR PLATING AND PLANARIZATION AND

PROCESS UTILIZING SAME. The disclosure of each U.S. Patent application mentioned above is incorporated by reference herein as non-essential subject matter. Additionally, the particular electrolyte chemistry of the modified plating solution disclosed in U.S. Patent application serial No. 09/544,558 will be described briefly here by way of example.

The modified plating solution referred to is formed from standard plating solution compositions that are modified to allow the deposition of a high quality Cu layer, and at the same time allow either simultaneous or sequential polishing and planarization of the deposited layer. The terms "electrolyte solution" and "plating solution" are used interchangeably throughout the following description. In this approach, commercially available, highly acidic Cu plating solutions are modified by the addition of oxidizers which do not appreciably affect the pH of the solution or the quality of the plated Cu layer. No slurry or particles are included in the formulation. Polishing and planarization is achieved using a fixed abrasive pad.

For plating, a potential is applied between an electrical contact to a substrate (e.g. a wafer) which is to be plated and an electrical contact to an anode assembly, making the substrate surface more negative than the anode assembly. The terms "substrate" and "wafer" are used interchangeably here. Under applied potential, a high quality layer of metal plates out of the

modified plating solution onto the wafer surface. By adjusting the gap between an abrasive polishing pad and the wafer surface and/or by adjusting the pressure with which the pad and the wafer surface touch each other, one can achieve just plating, or plating and polishing. For example, if there is a gap between the wafer surface and the pad, plating is expected to take place over the whole wafer surface as illustrated in Figure 2. In this case, a metal film is obtained that can be polished in a CMP process in a separate CMP machine. It should be noted that Cu layers plated out of the modified plating solutions were found to be polished more efficiently compared to Cu layers obtained from standard plating solutions and therefore are advantageous.

If the pad and the wafer surface are touching at low pressures, then plating can freely take place in the holes in the substrate where there is no physical contact between the wafer surface and the abrasive pad, but the plating rate will be reduced on the top surfaces where there is physical contact between the pad and the surface. The result is a metal deposit with uniform metal overburden across the surface of the substrate as shown in Figure 4. This is in contrast to the conventional deposit structure shown in Figure 2, where there is significant variation in metal overburden across the substrate. If the pressure with which the substrate and the pad surfaces touch each other is further increased, it is possible to obtain plating just in the holes or

features as shown in Figure 7. In this case, the increased polishing action on the high points of the substrate surface does not allow accumulation of the metal layer on these regions.

It is not fully understood how the addition of small amounts of oxidizers in the highly acidic Cu plating solutions allows the use of these solutions for plating and planarization. However, it is possible that the surface layer formed on the Cu deposit by the presence of oxidizers does not interfere with the plating of a good quality Cu layer, but at the same time can be efficiently removed from the sections of the film where the pad contacts it with some pressure.

The amount of oxidizer added to the plating solution may be less than 500 ppm; preferably, however, it should be more. Oxidizer concentration may typically be in the 0.01 wt.% to 10 wt.% range. Both inorganic and organic oxidizers, either pure or mixed, or their mixtures can be used as modifying agents, but organic oxidizers are preferred. Among the many organic oxidizers known to those in the field of chemistry, the preferred modifying agents are organic nitrites and nitrates. Although butyl nitrite is an organic oxidizer that was used as the modifying agent in the following examples, other modifying agents can also be used to obtain the same result. For example, other organic oxidizers, preferably organic nitrites, can be used. Organic nitrites include, but are not limited to, alkyl nitrites, aromatic nitrites,

and polyaromatic nitrites. Alkyl nitrites include, but are not limited to, primary, secondary and tertiary compounds of methyl, ethyl, propyl, butyl, and amyl nitrites. Additionally, nitrates of the above compounds may also be used.

Although the examples use Cu deposits, it should be understood that many other conductive materials such as Cu alloys, W, Au, Ni, Pt, Pd, Ag, Co, Sn, Pb and their alloys can be used.

EXAMPLE 1: STANDARD ELECTROLYTE SOLUTION

A Cu-sulfate based Cu plating solution was prepared as follows:

70 grams per liter of $CuSO_4+5H_2O$, 150 grams per liter of concentrated H_2SO_4, and 70 ppm per liter of Cl^- ions were mixed in enough water to make 10 liters of solution. Twenty-five ml of Ultrafill S2001®, 1.0 ml of Ultrafill A2001® from Shipley were then added to obtain a standard good quality plating electrolyte.

This solution was used for Cu plating on a 200 mm diameter wafer surface. The wafer surface contained sub-micron size features as well as features in the 10-100 micron range. The pad was a fixed abrasive pad supplied by 3M® company. The diameter of the pad was 180 mm and the anode assembly was oscillated in the horizontal direction so that plating could be achieved on all areas on the larger wafer surface. During plating, the distance between the pad and the wafer surface was kept at around 0.1 cm. The

plating current was 2 amperes and the plating solution flow was 5 liters/minute. The wafer was rotated at 75 rpm and the anode assembly with the pad was rotated at 100 rpm in the same direction. Several wafers were plated for times ranging from 90 seconds to 4 minutes. The Cu deposits after aging at room temperature for one day had a resistivity of below 2×10^{-6} ohm-cm, indicating good material quality.

EXAMPLE 2: POLISHING AND PLANARIZATION
USING STANDARD ELECTROLYTE SOLUTION

The plating experiment of Example 1 was repeated, except this time, after an initial period of 30 seconds, the pad was pushed against the wafer surface at a pressure of 1 psi for plating as well as polishing and planarization. The resulting Cu deposit had a rough surface with deep scratches apparently caused by the abrasive pad. There were also Cu particles smeared all over the surface of the wafer. Very little amount of material removal was achieved because material removed from one region of the surface by the action of the abrasive pad was probably deposited back onto the surface at another region in the form of smeared particles, which were welded or bonded to the substrate surface. The substrate defect level was extremely high and feature filling was poor.

EXAMPLE 3: MODIFIED ELECTROLYTE SOLUTION

Five ml per liter of butyl-nitrite were added as a modifying agent to the electrolyte of Example 1 and the plating and polishing experiment of Example 2 was repeated using this modified plating solution. The resulting Cu deposit was highly planar and was similar to the structure shown in Figure 4. Copper layer resistivity was still below 2×10^{-6} ohm-cm, demonstrating the ability of the modified electrolyte to yield high quality Cu deposits. The copper film was planar with uniform overburden over the sub-micron size features as well as the large features.

An anode assembly is disclosed in co-pending U.S. Patent application Serial No. 09/568,584, filed May 11, 2000, titled ANODE ASSEMBLY FOR PLATING AND PLANARIZING A CONDUCTIVE LAYER. A substrate holder/head assembly design is provided by co-pending U.S. Patent application serial No. 09/472,523, filed December 27, 1999, titled WORK PIECE CARRIER HEAD FOR PLATING AND POLISHING. The disclosures of these additional U.S. Patent applications are also incorporated by reference herein as non-essential subject matter.

The second step of the present invention is carried out in the same deposition chamber and in the same electrolyte, and involves inverting the polarity of the applied potential, i.e. voltage, thereby making the substrate surface more positive than the anode. The circuitry used for application and adjustment of the applied voltage, and for inverting the voltage polarity, is well known and

commonly used. Under these conditions, the already planar surface of the deposited material, such as the surface of the material shown in Figure 4, etches away, resulting in the structure shown in Figure 5. This structure has a thin Cu layer 8t over the surface of the patterned substrate which is flat and uniform on its surface (the upper surface in Figure 5). The thickness 8g of the Cu film 8t over the field regions may be one half to one tenth, and preferably is in a range of one third to one tenth, of its thickness 8h within the features. If the non-uniform conductive material deposit of Figure 2 were to be subjected to the same electro-etching step, the resulting structure would be non-uniform. Specifically, the material deposited in the large feature 1 would etch as much as the overburden. The resulting undesirable structure is shown in Figure 6.

It is possible to continue the electro-etching process that yields the structure of Figure 5 by extending the etching time and eventually obtain the structure shown in Figure 7. In this structure, the metal deposits in the patterned substrate features are physically isolated from each other. However, the barrier layer 3 still stands between the features and, therefore, electrical isolation of the Cu deposited in the features needs to be achieved through CMP or another process step that removes the barrier layer. The electro-polishing step can be monitored by monitoring the voltage-current characteristics of the electro-

etching process. The voltage-current characteristics are monitored using commonly known equipment (voltammeters, multimeters, voltmeters and ammeters, and so on). As the metal overburden is removed, the monitored voltage would rise (if etching is done under constant current conditions) because the conductivity of the barrier layer is lower than that of the metal overburden. If electropolishing were done under constant voltage conditions, which would be the preferred method, then a drop in the current would indicate that the overburden is removed. A combination of constant current/constant voltage approaches can be utilized for optimum control. The etching rate can also be manipulated by manipulating the voltage/current values during the process.

The structures depicted in Figures 5 and 7 are idealized versions of what happens in reality. In reality, the electro-polishing process carried out in the highly acidic Cu plating solution of our U.S. Patent application serial No. 09/544,558 mentioned above yields a Cu surface that is relatively rough, as can be seen in corresponding Figures 10 and 11. What is important, however, is the fact the overall surface of the overburden in Figure 10 is nearly uniform and, therefore, can be removed readily by a consequent CMP step. As for the structure in Figure 11, the rough nature of the surfaces may necessitate another planarization step which can easily be carried out in the same apparatus as will be discussed later.

One reason why prior art electro-polishing processes are carried out in special electro-polishing electrolytes is that when regular plating electrolytes are used for electro-polishing, they yield rough film surfaces. In this respect, it is more proper to refer to an electro-etching process such as the one we perform in our process as electrochemical etching or electro-etching rather than electro-polishing because the word "polishing" suggests that the resulting surface of the etched film is smooth and polished. Electro-polishing electrolytes may be high resistance and formulated using weak acids and special leveling additives to yield highly polished surfaces. Strong acids, such as phosphoric acid, neutral mineral salt solutions and their various combinations may also be used. Electrodeposition cannot be carried out with typical electro-polishing solutions. The unique feature of our invention is the use of the electroplating solution as the plating solution as well as the electro-etching solution in the same apparatus. The reason our invention can utilize the same solution for both plating and electro-etching is that our technique can planarize rough surfaces resulting from the electro-etching step, if necessary. We now will describe this unique feature.

After deposition of a planar film (Figure 4) and electro-etching in the same apparatus, a near-planar film such as the one shown in Figure 10 can be obtained. Although the surface of this film is not polished, the surface has global planarity over the

patterned substrate and the average thickness of the Cu overburden defined by the layer 8t' on the field regions is uniform. Therefore, a CMP step can be carried out on this substrate with relative rough surface morphology to obtain a structure similar to that shown in Figure 3, only with reduced dishing. The near-planar nature of the surface of the Cu film and thinness of the Cu film reduce dishing defects. Since the thickness of the Cu layer on the field regions of Figure 10 is small, the CMP step can be short and economical. In fact, a single CMP slurry that can remove both the thin Cu layer on the field regions and the barrier layer 3 can be used, and the structure of Figure 3, only with reduced dishing, can be obtained.

If the global uniformity of the etched Cu film on the patterned substrate of Figure 10 is not good, then a short plating step can be carried out in the ECMD apparatus to planarize the Cu film surface without increasing its thickness much. In this way, the surface quality and global uniformity of the film can be improved. This is a unique feature of the present invention. Multiple steps of plating and electro-etching processes can be carried out in the same apparatus, using the same electrolyte solution, to obtain the planar surface desired. In other words, even if the electro-etching step yields a rough surface morphology, this can be eliminated by a consequent, brief, ECMD step. Therefore, the structures shown in Figures 10 and 11 can be

converted into more idealized structures similar to those of Figures 5 and 7, respectively.

If the electro-etching time period is extended so that some etching is also done within the features (Figure 8), the over-etched areas can be plated again by changing the polarity of the applied voltage one more time (making the substrate voltage negative again with respect to the anode). Since the top surface of the substrate now has only the barrier layer 3 exposed over the field regions, deposition can selectively commence into the features, and it would be possible to get structures such as that depicted in Figure 9. The reason for this is that plating on the Cu in the features would be more efficient than plating on the barrier layer.

A structure such as the one shown in Figure 9 is very attractive for avoiding dishing defects during the CMP process. Typically, after the Cu deposition step, the substrates are heat treated (annealed) for grain growth. Certain examples of appropriate annealing processes are mentioned in commonly assigned, co-pending application serial no. 09/642,827, filed August 22, 2000, titled CONDUCTIVE STRUCTURE FABRICATION PROCESS USING NOVEL LAYERED STRUCTURE AND CONDUCTIVE STRUCTURE FABRICATED THEREBY FOR USE IN MULTI-LEVEL METALLIZATION, the disclosure of which is incorporated herein as non-essential subject matter. During this heat treatment step, the grains of Cu grow and its resistance gets

reduced. If a structure such as the one in Figure 7 or Figure 11 is heat treated and then polished using a CMP step to remove the barrier layer 3, the resulting structure, under non-ideal conditions, may show dishing of the large features as shown in Figure 3, only to reduced degree. One other problem may be that when a structure such as that shown in Figure 7 or Figure 11 is annealed, the size of the grains 10 of the Cu within the features may be relatively small and far from optimum (see Figure 12, which schematically shows the grain structure), especially if the thickness of the insulator 2 is small and, therefore, the depths of the features 1 and 1s are also small. However, when a structure such as that shown in Figure 9 is annealed before the CMP step, the grain size of the Cu within the features is expected to be larger (see Figure 13) because the thickness of the Cu deposits within and over the features is larger. A Cu deposit with large grain size and low resistivity is desirable in integrated circuit applications because lower resistance and large grains mean better electromigration properties and faster interconnection performance.

When the structure of either Figure 9 or Figure 13 is subjected to a CMP step for removal of the excess copper over the features as well as the barrier layer 3, a structure with little or no dishing can be obtained, as shown in Figure 14. The dramatic reductions of dishing defects and in the CMP time offered by the present invention are very attractive.

In other applications, the plated material deposited in the features of Figure 9 may be lead-tin solder alloys, tin, or solderable lead-free alloys such as SnCu, SnBi, or SnAg, ternary alloys, and so on. Instead of a CMP step, the substrate and plated material may be annealed to reflow the metal or alloy material and form the structure shown in Figure 15. After the reflow step, the barrier layer is removed by selective reactive ion etching (RIE) methods or by suitable wet etching methods to electrically isolate the deposits and form the structure shown in Figure 16.

In each embodiment of the invention described above, both the insulator layer 2 and the barrier layer 3 have conventional compositions such as those disclosed, for example, by U.S. patent 5,930,669 to Uzoh which names as the inventor one of the co-inventors of the subject matter of the present application. The insulator layer 2 may, for example, be composed of SiO_2 or another conventional dielectric material, while suitable materials that may be employed for the barrier layer 3 include, but are not limited to, Cr, Ti, TiN, W, Ta, TaN, TaN/Ta, Ta/TaN, Ta/TaN/Ta, TaN/Ti, Ta-Ti alloy, Ta-Cr alloy and Ti-Ta-Cr alloys.

In each of the embodiments described above, voltages are applied to electroplate at current densities of approximately 5-50 milliamperes per cm^2. Voltages are applied to obtain electro-etching, in each of the embodiments described, at current densities of approximately 0.1-20 milliamperes per cm^2. These ranges,

however, are not to be considered limiting.

The foregoing disclosure has been set forth merely to illustrate the invention and is not intended to be limiting. Since modifications of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and equivalents thereof.